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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/787,326	02/26/2004	Guenter Stenz	X-1478 US	3972

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EXAMINER	
SIEK, VUTHE	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 06/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/787,326	STENZ ET AL.	
	Examiner	Art Unit	
	Vuthe Siek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/787,326 filed on 2/26/2004. Claims 1-30 remain pending in the application.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1, 11 and 21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claim invention comprises two steps "identifying a cost function that penalizes floorplans..." and "annealing the circuit design to determine a floorplan using the cost function'. A cost function is not defined in the claim and using the cost function is ambiguous. Applicants are requested to clearly define these two steps and how they are interconnected.

The dependent claims are virtually rejected based on rejected based claims.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-30 are rejected under 35 U.S.C. 102(e) as being anticipated by Singh et al. (6,779,169 B1).

6. As to claims 1, 11 and 21, Singh et al. teach substantially the same invention. Singh et al. teach a method and apparatus for placement of components onto programmable logic device. The method comprising identifying a cost function (Fig. 12; col. 7 lines 30-60); defining modules comprising components of a same type (user defined logic regions, the user defined logic regions comprising components of same type; see summary; Fig. 1 shows different logic groups of components of same type); determining a set of shapes associated with at least one module (user may specify a size of logic region). The size of logic regions can be reshaped (Fig. 7). This suggests that a plurality of shapes can be generated accordingly. Singh et al. teach using simulated annealing teachniques to implement placement method (col. 7 lines 56-60) using the cost function and the set of shapes for the at least one module. The cost function associated with the move is evaluated. The cost function includes component that costs the move based on the logic regions' ability to meet timing constraints and on routing resources required by the logic regions. The cost function may utilize other parameters to cost the move. Singh et al. teach that a user has created hierarchies that include combinations of fixed-sized and automatically sized region. Singh et al. teach that preferred dimension (shape) of child logic region is reshaped such that it fits within its parent (col. 5 lies 25-38). The parent logic region is to be automatically sized (reshaped) in order to comply with fixed sizes of child logic regions. If the parent logic region includes primarily logic circuits, it would typically be sized to occupy a subset of a

Column. However, the sizing constraints for the child logic regions would make this assignment illegal. The preferred dimension of the parent logic region is reshaped to comply with the fixed dimensions of the chilled logic regions (col. 5 lines 39-50). Since, Singh et al. teach utilizing a cost function including parameters for the placement method of the logic regions having fixed and variable shapes (dimensions can be reshaped to make it fit), the cost function would penalize floorplan of the a circuit design that do not fit on the programmable logic device.

7. As to claims 2, 12 and 22, Singh et al. teach splitting modules into sub-modules, wherein at least one of the sub-modules consists of components of a same type (the size of logic regions is reshaped). The reshaped logic regions are splitted modules (sub-modules) (Figs. 5-6).

8. As to claims 3, 13 and 23, Singh et al. simulated annealing comprising assigning modules to a particular one of the set of shapes associated with that module (col. 5 lines 26-50).

9. As to claims 4, 14 and 24, Singh et al. teach simulated annealing comprising assign modules and assigned shapes to locations on the programmable logic device (Figs. 5-6; col. 5 lines 26-50).

10. As to claims 5, 15 and 25, Singh et al. teach swapping locations of components (Fig. 9, SWAP 1, SWAP 2).

11. As to claims 6, 16 and 26, Singh et al. teach simulating annealing comprising using bipartite matching of individual components. Fig. 1 shows LAB representing a number of LEs; MEGALAB representing a number of LABs; OCTANT representing a

number of MEGALABs; COLUMN representing a number of HALF; HALF representing a number of COLUMNs; and a CHIP (PLD) representing whole circuit design. As shown in the figure, individual components are matched components.

12. As to claims 7, 17 and 27, Singh et al. teach simulating annealing comprising identifying modules that share a timing critical path and moving identified modules closer to one another to satisfy timing constraint. Col. 7 lines 7-40 describes how identified logic regions that share a timing critical path and moving the identified modules closer to one another to satisfy timing constraints.

13. As to claims 8, 18 and 28, Singh et al. teach placement of components of a system onto programmable logic devices (PLDs) (see summary). A Field Programmable Gate Array is a common and known programmable logic device.

14. As to claims 9, 19 and 29, Fig. 1 shows each shape of a set of shapes associated with a module (logic region) has a minimum width and height of at least a width and height of a largest relatively placed module to be placed within that module (smallest size LEs to form LAB; LABs to form MEGALAB...).

15. As to claims 10, 20 and 30, Singh et al. teach generating a flat placement flow for the circuit design (initial placement by positioning components of a system onto a target device utilizing programmable logic devices); and a user is prompted to define a logic region that includes a subset of components of the system to be grouped together. A location is determined for the user defined region on the target device that allows the system to satisfy timing constraints. This placement method is performed utilizing

simulated annealing to measure a quality for the placement (floorplan) (see summary; Figs. 7, 12-13).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vuthe Siek whose telephone number is (571) 272-1906.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vuthe Siek

VUTHE SIEK
PRIMARY EXAMINER